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(54) Simulation of selected logic circuit designs.

(57) A system and method for selectively simulating logic circuit designs in which a data tables generator (12) receives information from a schematic entry program (10a) or netlist entry file (10b) and produces data tables for use by a simulator (14). A designer provides inputs to the data tables generator from a schematic entry program or a netlist entry file. The data tables generator (12) generates from the information received a table of used integrated circuits and a table of their connections. A simulator (14) then receives the output from the data tables generator (12) and produces a design simulation program table that executes integrated circuit model subroutines stored in an integrated circuit model reference library (4) and netlist subroutines stored in a netlist connectivity table (18). The system may also be used for testing logic circuits on a printed circuit board by capturing signals from a potentially defective logic section of the printed circuit board and feeding them into test points of the integrated circuit simulated by the computer simulator.

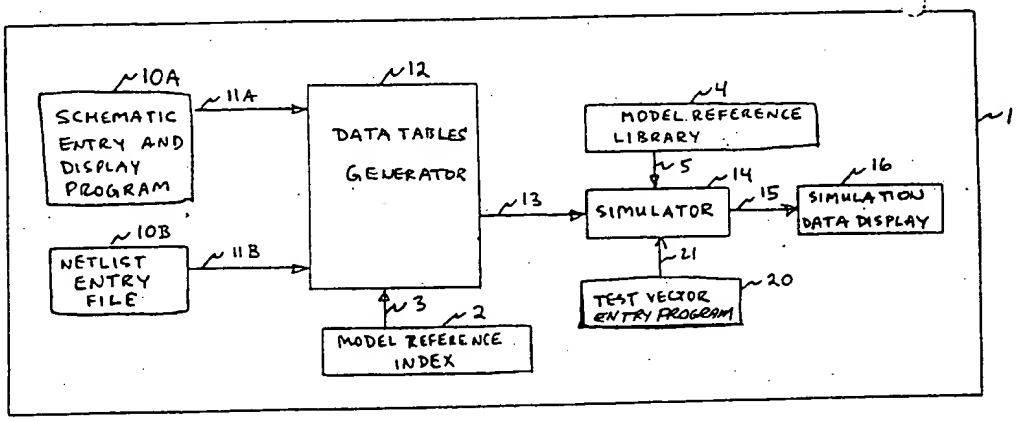

FIG. 1

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EUROPEAN SEARCH REPORT

Application Number

EP 90 30 6621

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	US-A-4 827 427 (HYDUKE) 2 May 1989	1,11,12, 15,17	G06F15/60
Y	* column 1, line 55 - line 58 *	13,14,16	
A	* column 2, line 17 - column 4, line 25; figures 1,2 *	2,4,5,8, 9	

Y	ELECTRONIC DESIGN. vol. 36, no. 3, March 1988, CLEVELAND OH US pages 50 - 58; MILNE: 'electronic design report - Logic simulation on personal computers : Friend or foe?'	13,14	
A	* page 55, column 3, line 15 - line 33; figures 3-4 *	1,3-5, 9-12,15, 17	

Y	US-A-4 791 357 (HYDUKE) 13 December 1988	16	
A	* column 1, line 22 - line 26 *	5-7, 9-11,15, 17	
	* column 3, line 14 - line 41; figure 1 *		TECHNICAL FIELDS SEARCHED (Int. Cl.5)

A	INTEGRATION, THE VLSI JOURNAL. vol. 7, no. 1, April 1989, AMSTERDAM NL pages 21 - 34; HWANG: 'incremental algorithms for digital simulation' * page 23, line 23 - page 27, line 4; figures 2-4 *	1,2,12	G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	06 AUGUST 1992	GUINGALE A.

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